Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A processor for use in a Voice-over-Internet Protocol telephone, including:

an internal bus for routing of signals in the processor;

a ~~Voice-over-Internet Protocol~~ processing core to control the processor ~~core operable~~ to transmit computer data and voice data over a computer network, the processor core including one or more pipelines to execute instructions, the processing core directly coupled to the internal bus;

~~a bus on which signals internal to the processor are routed;~~

an on-chip memory directly coupled to ~~the Voice-over-Internet Protocol processor core through~~ the internal bus and separate from the processing core, the on-chip memory including a program memory to include instruction for execution by the processing core and a data memory to store cache for the ~~processor core~~ processing core;

a pulse code modulation (PCM) interface directly coupled to the internal bus and separate from the processing core and on-chip memory, the PCM interface including a PCM communication port for connection to an external voice codec;

~~one or more communication ports coupled to the Voice-over-Internet Protocol processor core and memory through the bus;~~

an Ethernet interface directly coupled to the internal bus and separate from the processing core, on-chip memory and PCM interface, the Ethernet interface including a repeater, ~~coupled to the Voice-over-Internet Protocol processor core through the bus; and~~ one or more IEEE 802.3 media access controllers (MACs) and an Ethernet port for connection to an external network; ~~coupled to the Voice-over- Internet Protocol processor core through the bus, the one or more MACs being separate from the Voice-over-Internet Protocol processor core, wherein the Voice-~~

~~over-Internet Protocol processor core transmits the computer data and the voice data through the one or more communication ports, and wherein the repeater one or more communication ports and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core~~

an external bus unit directly coupled to the internal bus and separate from the processing core, on-chip memory, PCM interface and Ethernet interface, the external bus unit providing a bridge for connection through a device bus, other than the external network, to an external memory,

wherein the instructions are configured such that when executed by the CPU,

PCM coded speech data received by the PCM interface is transported to the external memory, read from the external memory by the processing core and compressed by the processing core and written back to the external memory, and voice data packets with such speech data are read from the external memory and forwarded to the 802.3 MAC and fed into the external network by the repeater, and

voice data packets received by the Ethernet interface are transported to the external memory, read from the external memory by the processing core and decompressed by the processing core and written back to the external memory, and PCM coded speech data from the received voice data packets is transported by the PCM interface to the external voice codec,

and wherein the internal bus, processing core, on-chip memory, PCM interface, Ethernet interface, and the external bus unit are integrated into a single chip.

2-3. (Cancelled)

4. (Currently Amended) The processor of claim 1, ~~wherein the one or more communication ports further include~~ further comprising one or more universal serial bus (USB) ports.

5. (Currently Amended) The processor of claim 1, wherein ~~the~~ one or more communication ports allow the ~~Voice-over-Internet Protocol~~ processor core to be coupled to one or more external components without external interfacing circuitry.

6-8. (Cancelled)

9. (Currently Amended) The ~~apparatus~~ processor of claim [[8]] 1, wherein each ~~PCM~~ Ethernet port is operable to handle up to 30 time slots, and wherein each time slot is capable of handling a 64K bit/sec voice channel.

10-18. (Cancelled)

19. (Previously Presented) The processor of claim 1, wherein at least one pipeline supports one of arithmetic, load and store, and loop control operations for the processor core.

20. (Previously Presented) The processor of claim 1, wherein at least one pipeline is configured to execute at least one of integer instructions, bit operations, MAC instructions and conditional data jumps.

21. (Currently Amended) The processor of claim 1, wherein at least one pipeline is configured to execute [[s]] load and store instructions, context operations, system instructions, address arithmetic and conditional and unconditional address instructions for the processor core.

22. (Previously Presented) The processor of claim 1, wherein at least one pipeline includes a loop hardware cache buffer operable to store location, target and minimal set of information required to execute repetitive loop within the at least one pipeline so as to achieve loop optimization.

23. (Currently Amended) The processor of claim 1, wherein the processor core includes separate address and data buses for the program memory and the data memory.

24. (Cancelled)

25. (New) The processor of claim 1, wherein the internal bus is a flexible peripheral interconnect (FPI) bus.

26. (New) The processor of claim 25, wherein the FPI bus is a demultiplexed, pipelined bus.